

LISTING OF CLAIMS:

This listing of claims will replace all prior version, and listings, of claims in the application:

Claims 1-8 (canceled).

9. (Previously Presented) A method for serially transmitting data between a first station and a second station, comprising:

transmitting in parallel at least two signals unidirectionally on at least two signal paths, wherein the first station has a first shift register and the second station has a second shift register, each of the first and the second shift registers having at least two register cells corresponding to the at least two signal paths, the at least two signals being routed in parallel on the at least two signal paths into the at least two register cells of the first shift register;

transmitting data corresponding to the at least two signals serially from the first shift register to the second shift register by automatically clocking the register cells of the first shift register and the second shift register from a time base directly connected to the register cells, wherein the first shift register and the second shift register are connected by a serial interface, whereby transmission of the at least two signals occurs in real time, wherein each transmitting is performed without loading a CPU.

10. (Previously Presented) The method as recited in Claim 9, wherein the automatic clocking of the first and second shift registers is performed by a time base of the first station such that the first shift register receives a clock signal of the time base and the first shift register automatically transmits the data corresponding to the at least two signals with the aid of the clock signal.

11. (Previously Presented) The method as recited in Claim 9, wherein the automatic clocking is performed at a clock-pulse rate that is at least twice as high as a signal rate that results from a resolution of a signal having the higher resolution between the at least two signals.

12. (Previously Presented) The method as recited in Claim 9, wherein the at least two signals are pulse-width modulated signals.

13. (Previously Presented) The method as recited in Claim 9, wherein the at least two signals each have a high signal level and a low signal level, and wherein the high signal levels of the at least two signals being substantially equal, and wherein the low signal levels of the at least two signals being substantially equal.

14. (Previously Presented) The method as recited in Claim 9, wherein the automatic clocking occurs at a clock-pulse rate, and a cycle time resulting from the clock-pulse rate is one of less than and equal to a slope time of the at least two signals transmitted.

15. (Previously Presented) A system for serially transmitting data between a first and a second station, comprising:

- a first station having a first shift register with at least two register cells;
- a second station having a second shift register with at least two register cells;
- a serial interface connecting the first shift register and the second shift register; and
- a time base directly connected to the register cells of the first and second shift registers;

wherein at least two signals are unidirectionally routed in parallel on at least two signal paths into the at least two register cells of the first shift register, and wherein data corresponding to the at least two signals are serially transmitted from the first shift register to the second shift register by automatically clocking the register cells of the first shift register and the second shift register from the time base, whereby transmission of the at least two signals occurs in real time and are performed without loading a CPU.

16. (Previously Presented) The system as recited in Claim 15, wherein the time base is a timer module that automatically generates a time signal at fixed intervals.